Circuit Theory and Design of Power Factor Correction Power Supplies

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Contents

We will re-examine the concept of power factor correction (PFC), starting from the basics of circuit theory.

We will consider the fundamental requirements of PFC and how such requirements can be fulfilled.

We will develop systematic procedures for synthesizing PFC power supplies.

Introduction

- Efficient and compact power supplies are not priceless.
  - They present themselves as nonlinear loads to the mains, drawing current of distorted waveforms;
  - The generate noise that interferes other equipment and the environment
- Quantitative measures of power quality
  - Power factor / harmonic distortions
  - Radiated and conducted EMI

Power Factor

$$\text{p.f.} = \frac{\text{Actual Power}}{VI \text{ Product}}$$

$$= (\text{displacement factor})(\text{distortion factor})$$

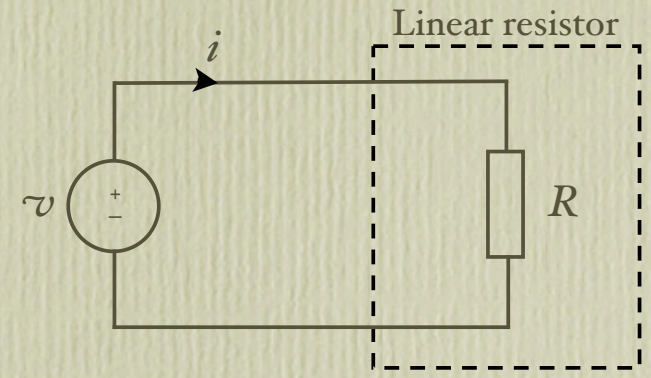
Phase shift between v and i — Harmonic contents in i

Old concept of renewed interest

$$\text{p.f.} = \underbrace{\cos\phi}_{\text{displacement factor}} \times \underbrace{\sqrt{\frac{1}{1 + (I_2/I_1)^2 + (I_3/I_1)^2 + \cdots}}}_{\text{distortion factor}} = \frac{\cos\phi}{\sqrt{1 + \text{THD}^2}}$$

Power Factor Correction

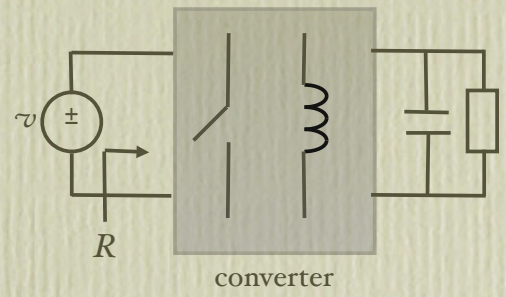
Technique:
Power
Factor
Correction



- Power converters are required to present themselves as linear resistance to the supply voltage. If the input voltage, *v,* is a sine wave, so is the input current, *i*.

Power Converters Fundamentals

The question is:
How to make the converter look resistive?



- Composed of inductors and switches as seen from the mains;
- Operating with switches turned on and off at a frequency much higher than 50 Hz.

Hints

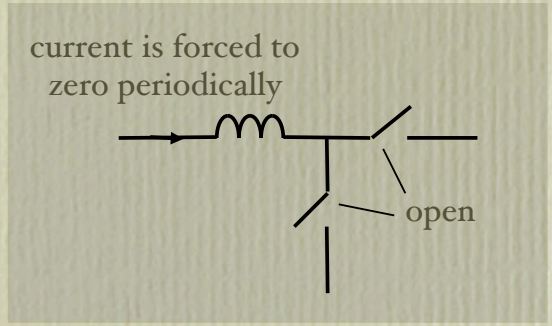
- The converter does not need to be resistive for all frequencies.
- If a filter is already there to remove switching frequency ripples, the converter needs only be resistive at low frequencies.

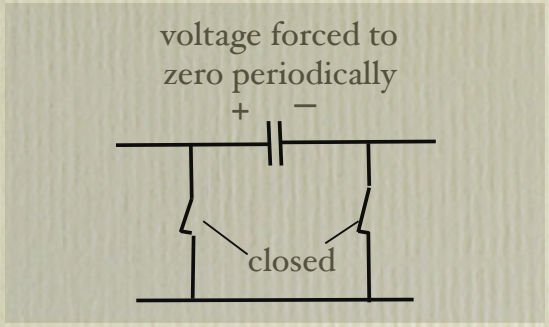
Afterall, ***power factor correction is a low-frequency requirement.***

Destruction of Dynamics

Fundamental Properties

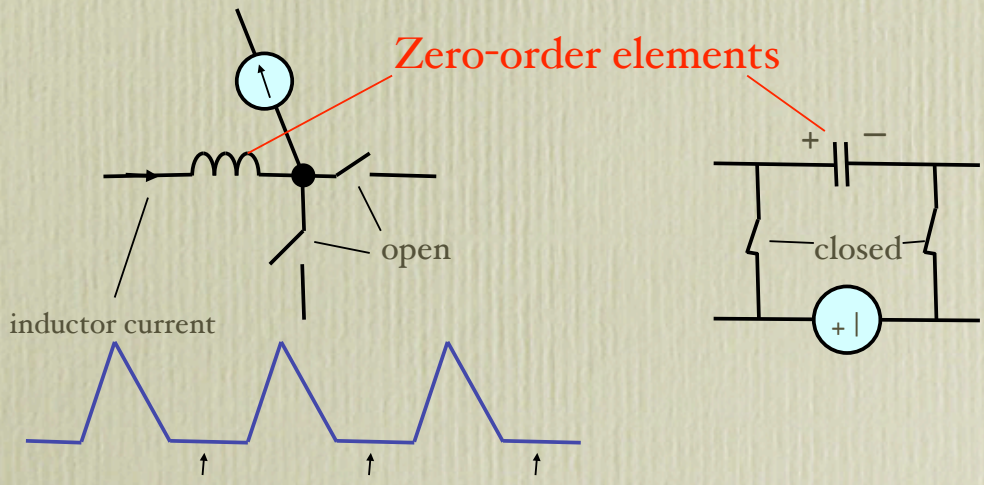
- Inductors cannot (are not allowed to) have “jump” current
- Capacitors cannot (are not allowed to) have “jump” voltage





Zero-order Inductors/ Capacitors

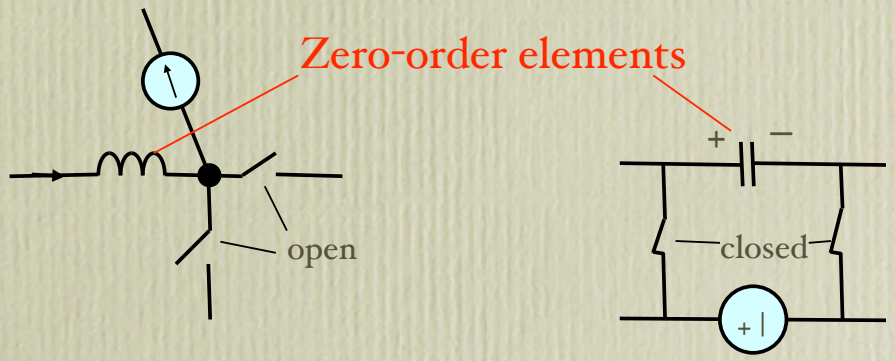
- Inductors forming a cutset with open switch(es) and/or current source(s) periodically
- Capacitors forming a loop with closed switch(es) and/or voltages source(s) periodically



i_L = zero periodically ⇒ no dynamics!

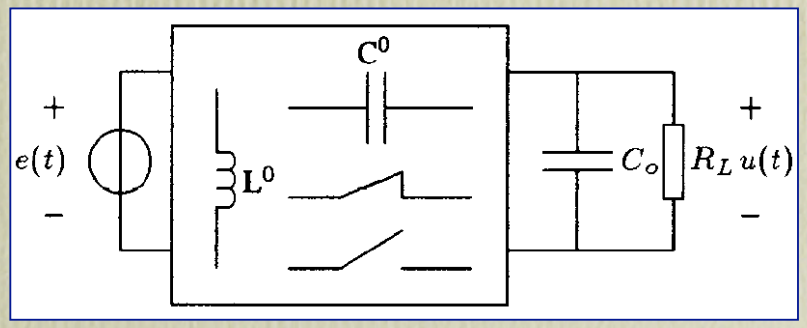
Devoid of Dynamics

- Zero-order elements (Lo or Co) obviously do not store energy in a cycle, and hence are devoid of low-frequency dynamics. They can be considered as ***being resistive*** in the low-frequency range.



First Idea

- If the converter
  - contains only zero-order elements; and
  - the input does not "see" the output at all times,
- then the converter will look resistive to the input.
- Thus, we can make a PFC converter from this idea.



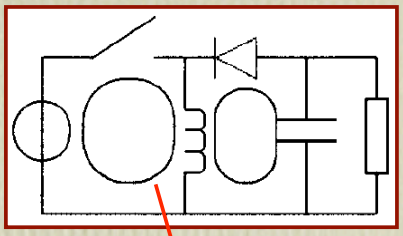
The "Perfect" Solution

Consider a **flyback or buck-boost converter**.

First, we can see that the input never "see" the output.

So, if we make the inductor zero-order by operating it in **DCM**, we have a resistive input.

DCM operation



forming cutset with open switches periodically

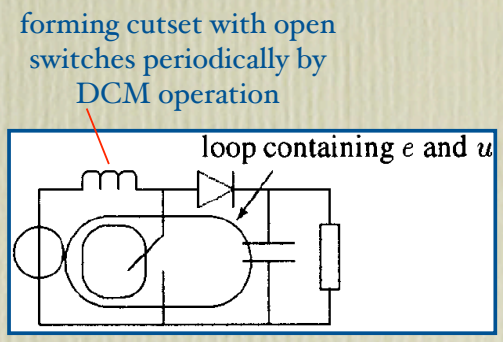
Applying simple averaging, input resistance is $R_{\text{in}} = \dfrac{2L}{D^2 T}$

A Not-So-"Perfect" Solution

Consider a **boost converter**.

Observe that the input sometimes "see" the output!!

Even if we make the inductor zero-order by operating it in **DCM**, we don't precisely have a resistive input.



Applying simple averaging, input resistance is $R_{\text{in}} = \dfrac{2L}{D^2T}\left(1 - \dfrac{V_{\text{in}}}{V_o}\right)$

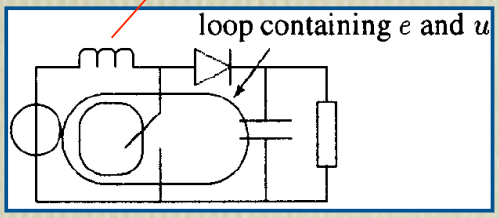
"Perfecting" It!

Consider a **boost converter** again.

If D is reserved for other purposes, the T must be varied to achieve "perfect" PFC, as in SSIPP*. (See Chow *et al.*, 1997)
It was also shown (Redl *et al.* and others) that even if no control is used, the power factor attained is still pretty "good"—good enough!

*SSIPP—single-stage single-switch isolated PFC power supply

forming cutset with open switches periodically by DCM operation



$$R_{\text{in}} = \frac{2L}{D^2T}\left(1 - \frac{V_{\text{in}}}{V_{\text{o}}}\right)$$

variable

Feedback feedforward

What do we know now?

Basic Criteria:

- The DCM buck-boost or flyback converter satisfies the basic criteria of a "perfect" PFC. It thus naturally gives a good p.f.
- The DCM boost and buck converters are "not-so-perfect", but can theoretically be perfected via feedback/feedforward.

Other Practical Considerations:

- The DCM boost converter is preferred for its relatively better efficiency.
- Even under no control, the DCM boost converter has a pretty "good" p.f.
- The DCM buck converter is not preferred for its high peak current, and it suffers from the low voltage blackout (because it is a buck)!

Other Possibilities

Our fundamental criterion is

Destruction of Dynamics of L and C!

For voltage converters, the main constituent is the switching L. Therefore, our basic wish is to destroy the dynamics of the L in the converter.

We have shown how this destruction can be done by DCM operation.
What else can we do?

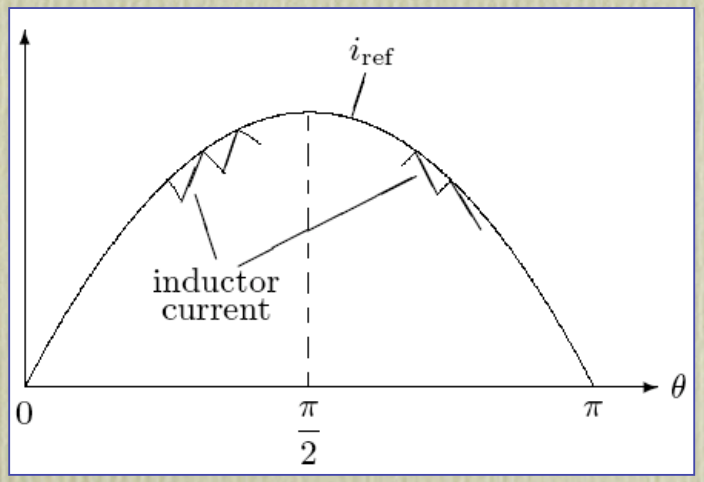
Direct Destruction

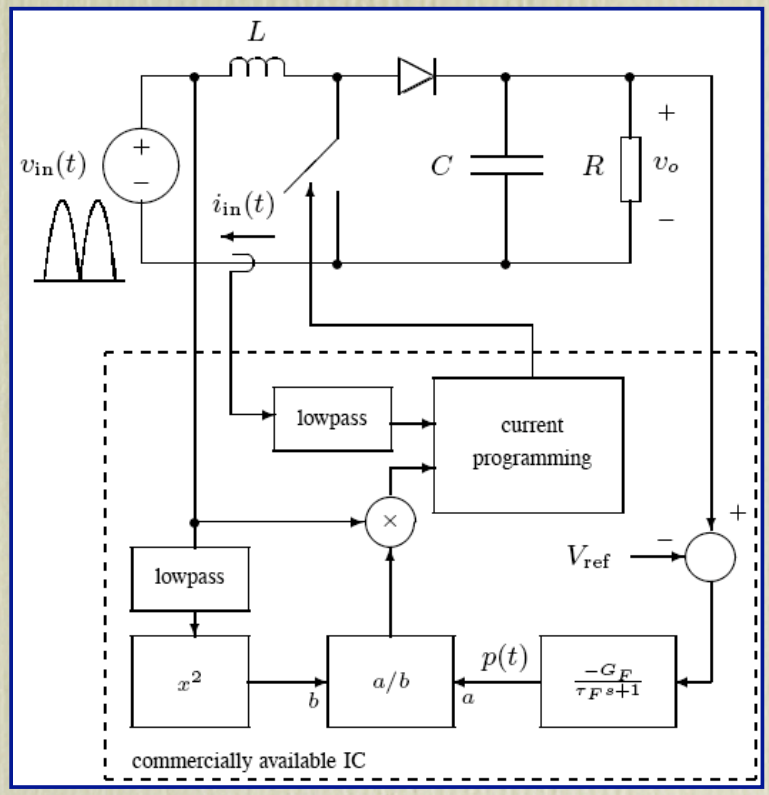
Using direct current-programming, we can destroy the dynamics of the L. (The idea is that if we make the current dependent on the output voltage, it is no longer an independent variable, hence it is devoid of dynamics!)

Specifically, we program the current of L such that it assumes the wave shape that we want.

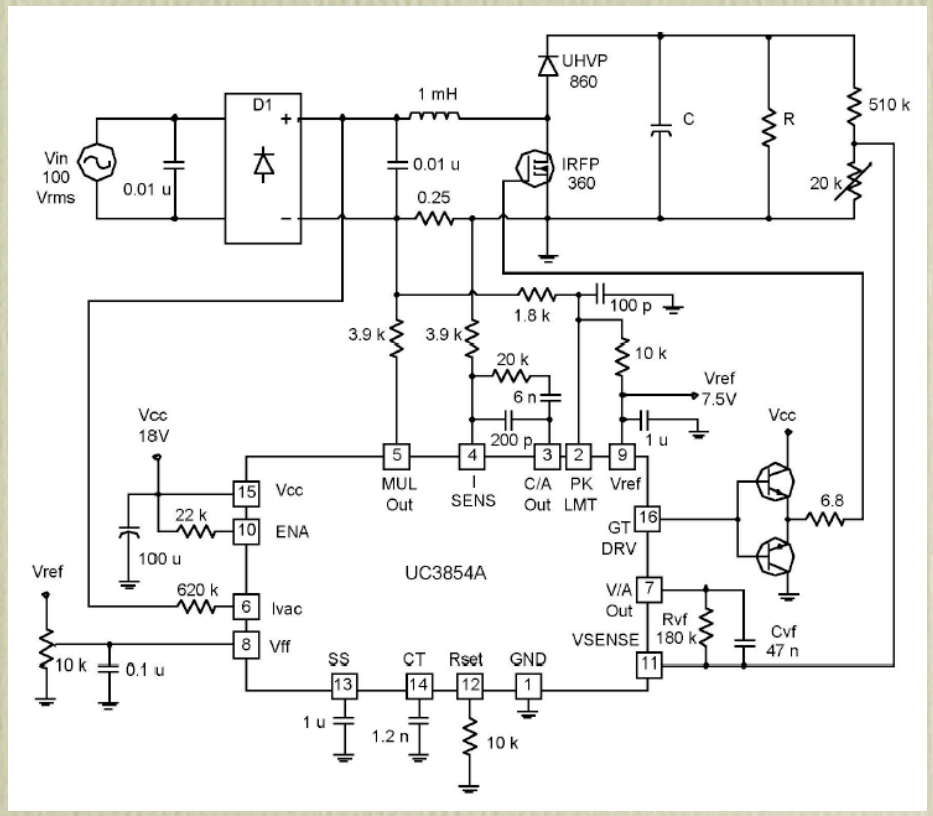
Second Idea

- CCM operation of the boost converter.
- Direct current programming such that its average (ripple removed) waveshape follows the input.





Standard IC Implementation



e.g., ACM PFC IC controller (see Wong, Tse & Tang in PESC2004)

Other Ideas

We have considered zero-order L.

How about zero-order C?

The problem (of course) is the basic restriction of

- the supply being a voltage
- the usual load requiring a voltage

(That's why all converters are switching inductors in practice.)

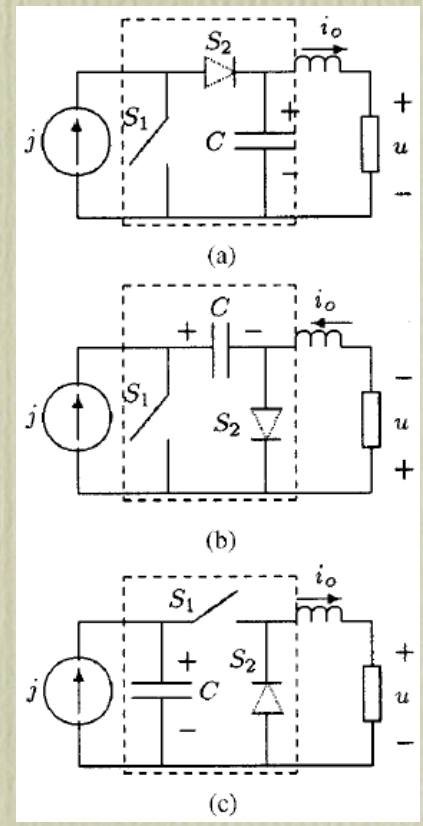
Theoretically, switching capacitors are never excluded!

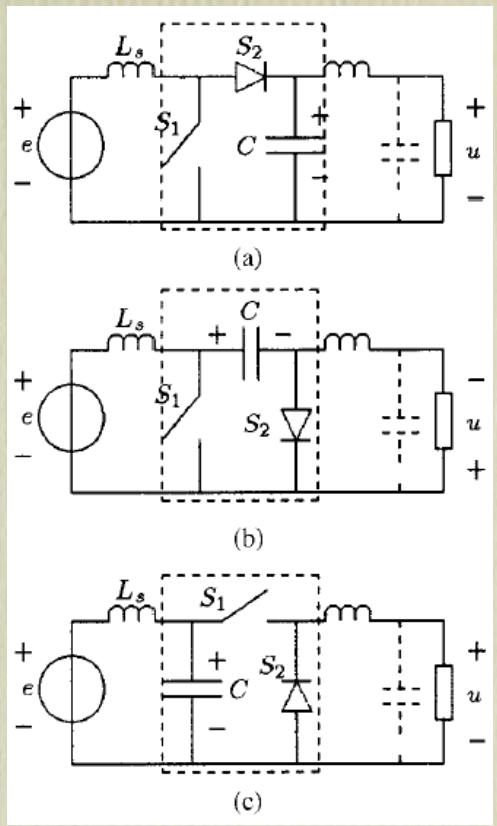
Duality Derivation

dual of
DCM buck

dual of
DCM buck-boost

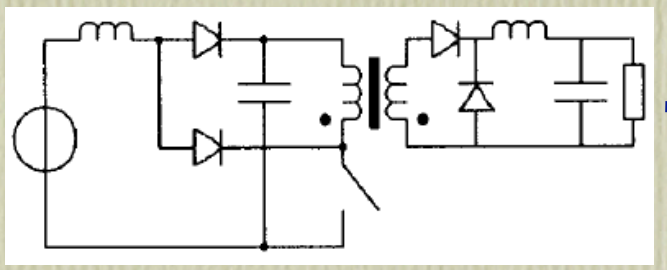
dual of
DCM boost



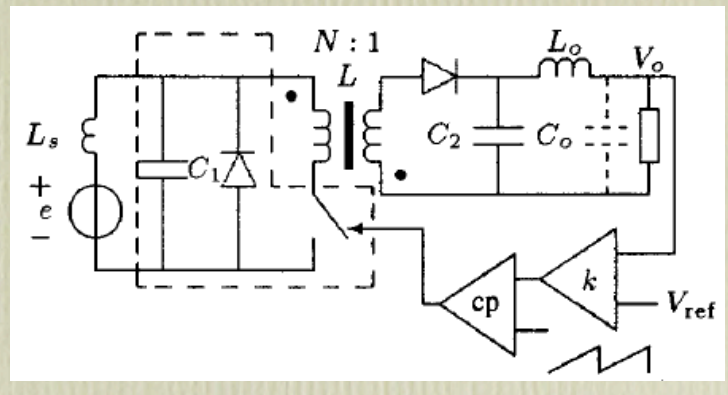


e.g. Duality Derived SSIPP

SSIPP based on boost + buck cascade



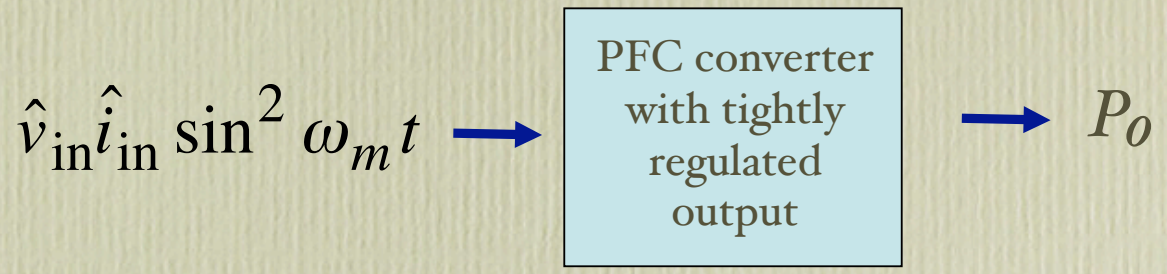
exact dual



For detailed analysis and experiments, see
C. K. Tse, Y. M. Lai, R. J. Xie and M. H. L. Chow, "Application of Duality Principle to Synthesis of Single-Stage Power-Factor-Correction Voltage Regulators," *International Journal of Circuit Theory and Applications,* vol. 31, no. 6, pp. 555-570, November 2003.

Numerous possibilities exist within this theoretical framework!

Practical PFC System



Always require tightly regulated DC output, in addition to PFC.

Can one converter do the jobs of PFC and tight output regulation?

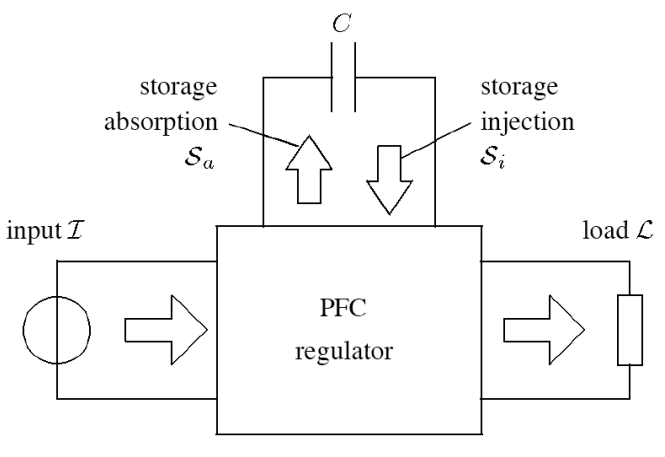
No!

because we need a low-freq power buffer!

Power Buffer

In general we need a power buffer to achieve PFC and tight output regulation simultaneously.

3-port model



How many basic converters do we need?

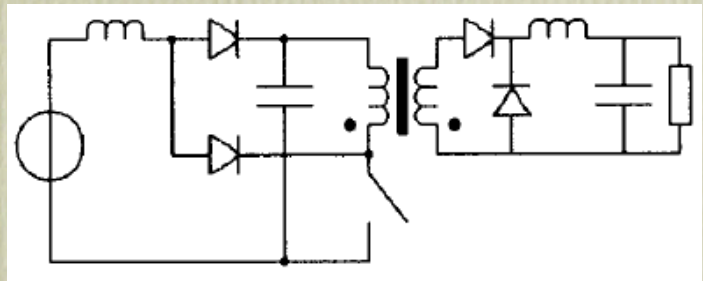
Answer: TWO.
(For a rigorous proof, see
C. K. Tse and M. H. L. Chow, "Theoretical study of Switching Converters with Power Factor Correction and Voltage Regulation," *IEEE Transactions on Circuits and Systems I,* vol. 47, no. 7, pp. 1047-1055, July 2000.)

Two is enough!

We need two converters (arranged suitably, of course).

In fact, the so-called single-stage PFC regulator has **two** converter stages, strictly speaking. For example, the SSIPP is a boost converter plus a buck converter.

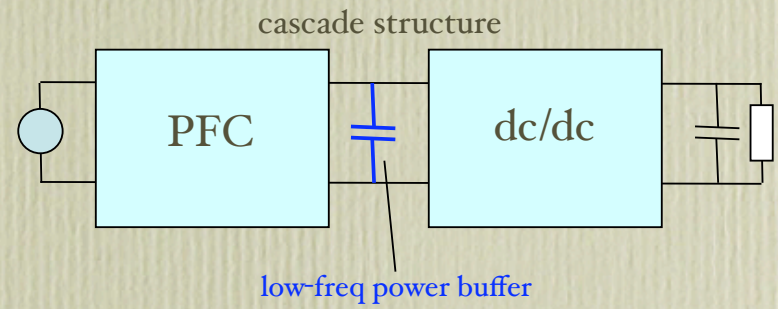
SSIPP by Redl *et al.*



A Different Question

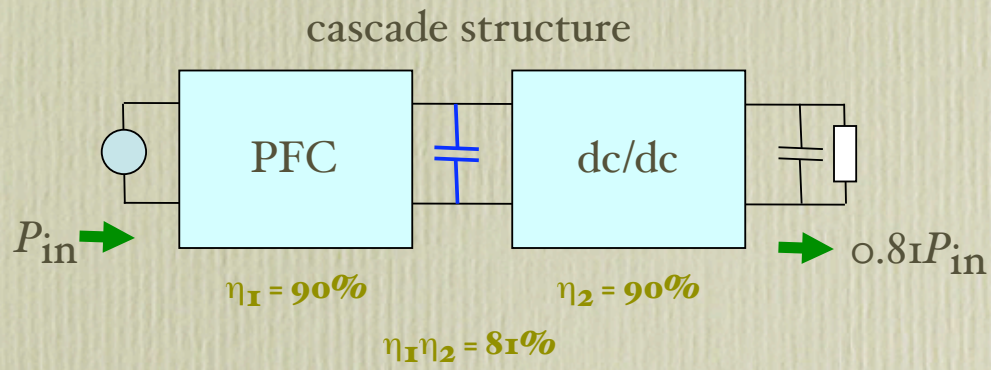
Probably, the question of interest to the engineers is *HOW THE TWO CONVERTERS ARE POSSIBLY ARRANGED?*

Best known configuration:



Cascade Structure

Obviously, the problem of the cascade structure is the double processing of power in the two stages, degrading the efficiency.

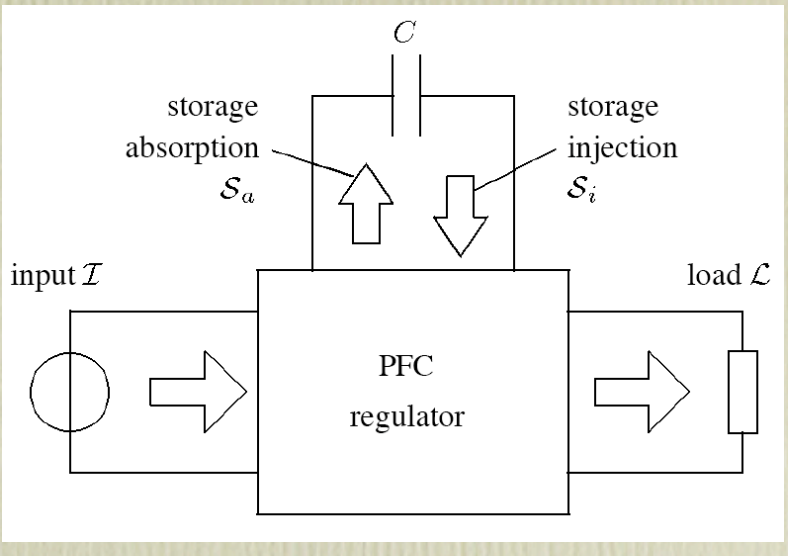


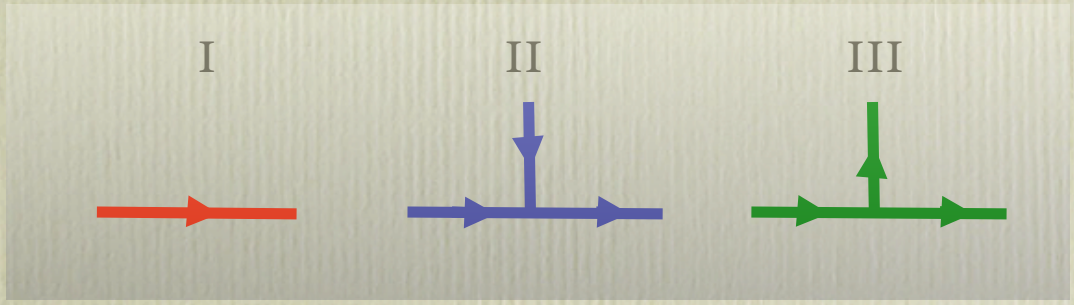
Naturally, we wish to examine the way power is being processed.

Power Processing

Let's start from the basics again.

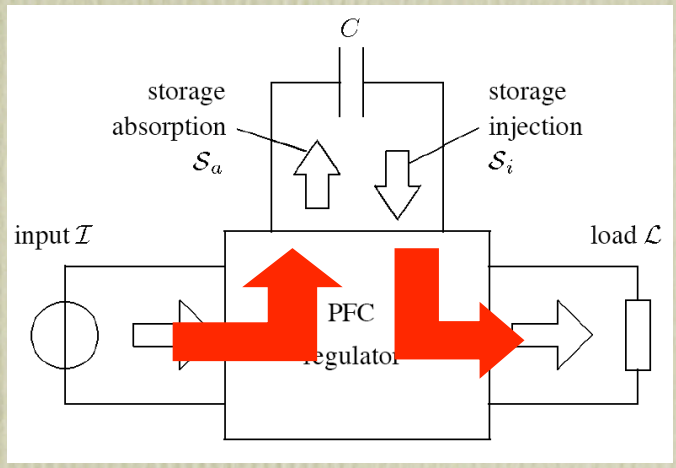
In what ways power can flow within the 3-port model?





Power Processing

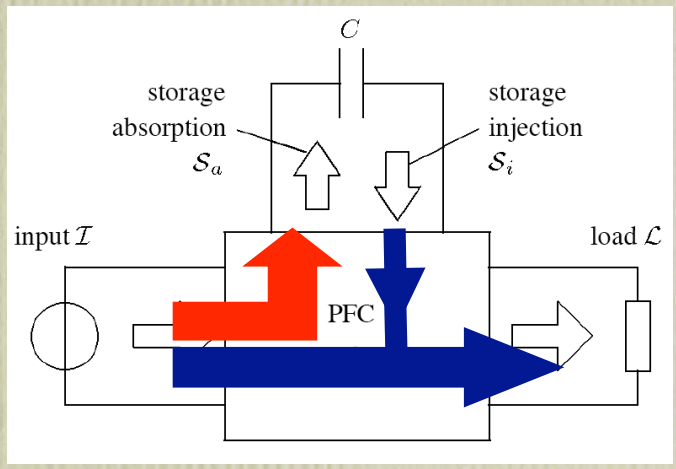
Let's try fitting in the three types of flows.



Type I and Type I

Power Processing

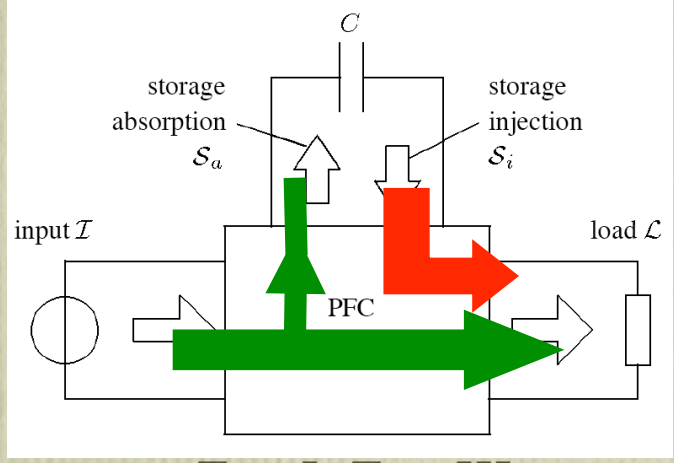
Another try!



Type I , Type II

Power Processing

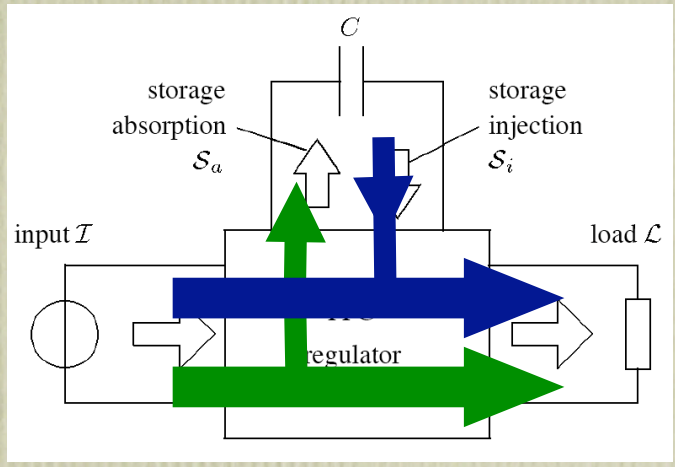
Another try!



Type I , Type III

Power Processing

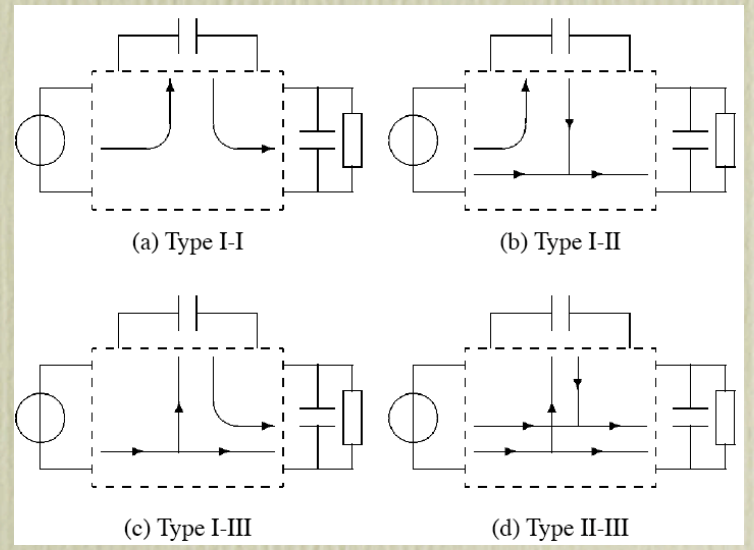
Another try!



Type II , Type III

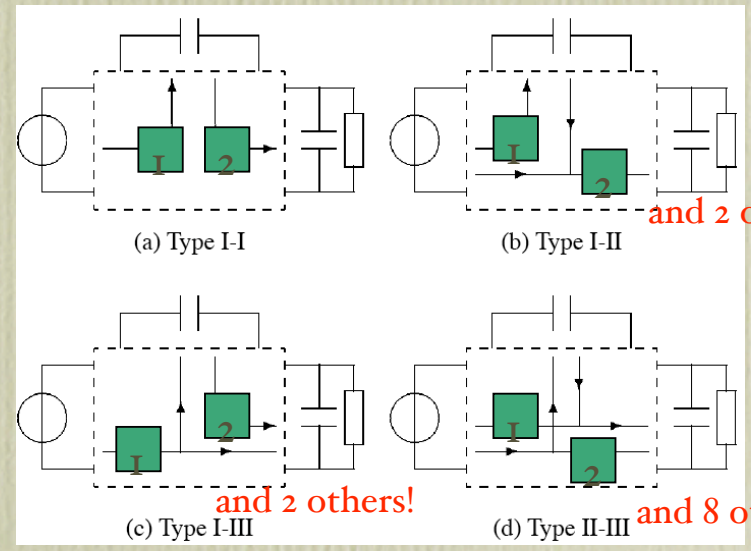
Power Processing Possibilities

To fulfill the power flow conditions of the 3-port model, we have 4 power flow possibilities.



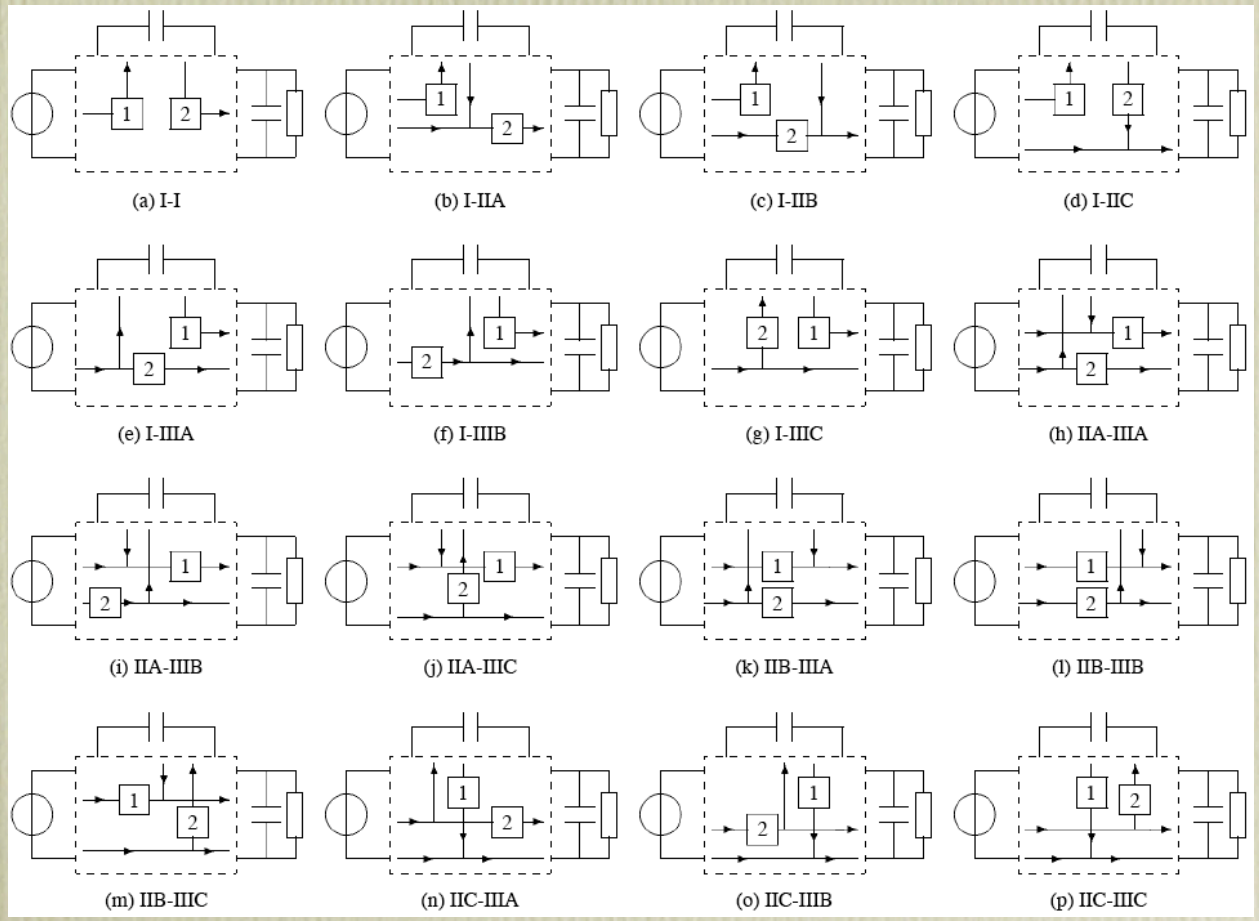
Completing the Structure

Finally, we place 1 converter to each path.



The Sixteen Configurations

Fitting in the two basic converters, we clearly see 16 possible structures.

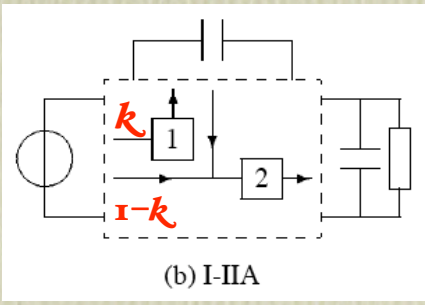


Theoretical Efficiency

We can theoretically compare the efficiencies of the 16 structures. Obviously, the cascade (type I-I) is the poorest, and the others are always better since power is not doubly processed.

For example, consider the I-IIA structure.
Suppose k is the ratio of power split.

$$\begin{aligned}\text{efficiency} &= k\eta_1\eta_2 + (1-k)\eta_2 \\ &= \eta_1\eta_2 + (1-k)\eta_1(1-\eta_2) \\ &> \eta_1\eta_2\end{aligned}$$



(b) I-IIA

We shall see that this k is a very important parameter. If k is too large, the circuit resembles the cascade structure, hence no efficiency advantage. But if it is too small, P.F. degrades.

Theoretical Efficiency

We can theoretically compare the efficiencies of the 16 structures. Obviously, the cascade (type I-I) is the poorest, and the others are always better since power is not doubly processed.

Config.	Efficiency	
I-I	$\eta_1\eta_2$	
I-IIA	$\eta_1\eta_2+(1-k)\eta_2(1-\eta_1)$	where $(1-k)\eta_2(1-\eta_1)>0$
I-IIB	$k\eta_1+(1-k)\eta_2$	where $k\eta_1+(1-k)\eta_2>\min\{\eta_1,\eta_2\}>\eta_1\eta_2$
I-IIC	$\eta_1\eta_2+(1-k)(1-\eta_1\eta_2)$	where $(1-k)(1-\eta_1\eta_2)>0$
I-IIIA	$k\eta_1+(1-k)\eta_2$	same as I-IIB
I-IIIB	$\eta_1\eta_2+(1-k)\eta_2(1-\eta_1)$	same as I-IIA
I-IIIC	$\eta_1\eta_2+(1-k)(1-\eta_1\eta_2)$	same as I-IIC
IIA-IIIA	$k\eta_1+(1-k)\eta_2$	same as I-IIB
IIA-IIIB	$\eta_1\eta_2+m(1-k)\eta_2(1-\eta_1)+k\eta_1(1-\eta_2)$	where $m(1-k)\eta_2(1-\eta_1)+k\eta_1(1-\eta_2)>0$
IIA-IIIC	$\eta_1\eta_2+m(1-k)(1-\eta_1\eta_2)+k\eta_1(1-\eta_2)$	where $m(1-k)(1-\eta_1\eta_2)+k\eta_1(1-\eta_2)>0$
IIB-IIIA	$\eta_1\eta_2+\eta_1\eta_2[\frac{km}{\eta_1}(\frac{1}{\eta_2}-1)+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	where $(1-k)\eta_1+k\eta_2>\eta_1\eta_2$ (see I-IIB)
IIB-IIIB	$k\eta_1+(1-k)\eta_2$	same as I-IIB
IIB-IIIC	$\eta_1\eta_2+\eta_1\eta_2[\frac{km}{\eta_1}(\frac{1}{\eta_2}-1)+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	where $(1-k)\eta_1+k\eta_2>\eta_1\eta_2$ (see I-IIB)
IIC-IIIA	$\eta_1\eta_2+\eta_1\eta_2[\frac{(1-k)\eta'+k\eta_1\eta_2}{(\eta_1\eta_2)\eta'}-1]$	where $\eta'=\frac{\eta_1\eta_2}{(1-m)\eta_1+m\eta_2}$ and $(1-k)\eta'+k\eta_1\eta_2>\eta_1\eta_2\eta'$
IIC-IIIB	$\eta_1\eta_2+\eta_1\eta_2[k+(\frac{(1-k)\eta_2+k\eta''}{\eta_2\eta''}-1)]$	where $\eta''=\eta_1\eta_2$ and $(1-k)\eta_2+k\eta''>\eta_2\eta''$
IIC-IIIC	$\eta_1\eta_2+(1-km)(1-\eta_1\eta_2)$	where $(1-km)(1-\eta_1\eta_2)>0$

Comparing Efficiency

Note:

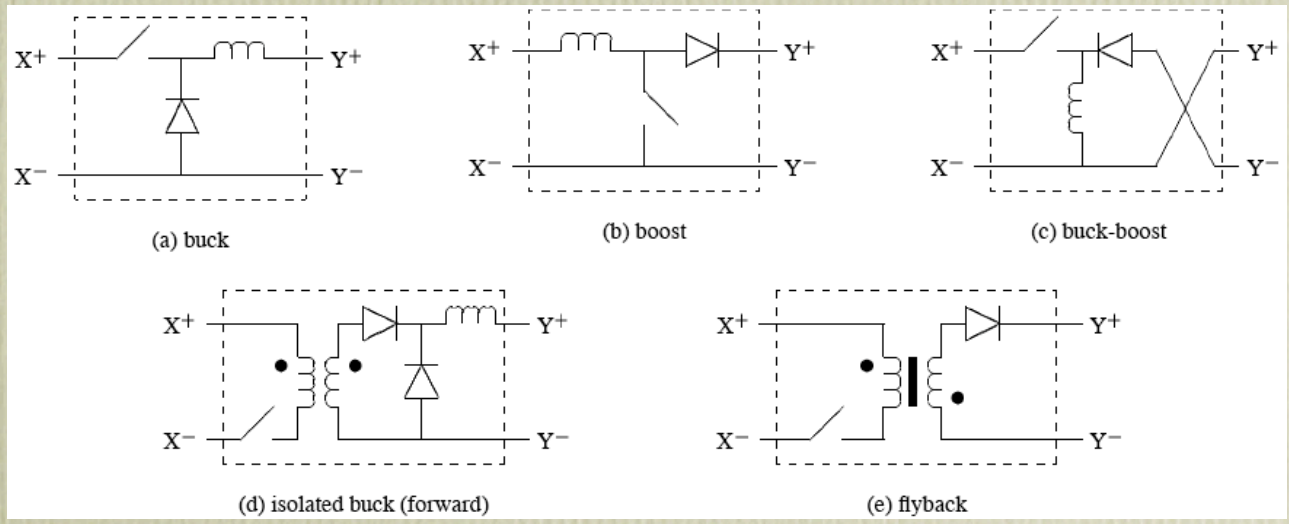
I don't mean the above efficiency comparison is absolute! That will always put me in endless debate! You may have different efficiency optimization schemes for different stages, and in different forms.

So, why should I bother here?

Synthesis

The most important problem is HOW TO CREATE CIRCUITS.

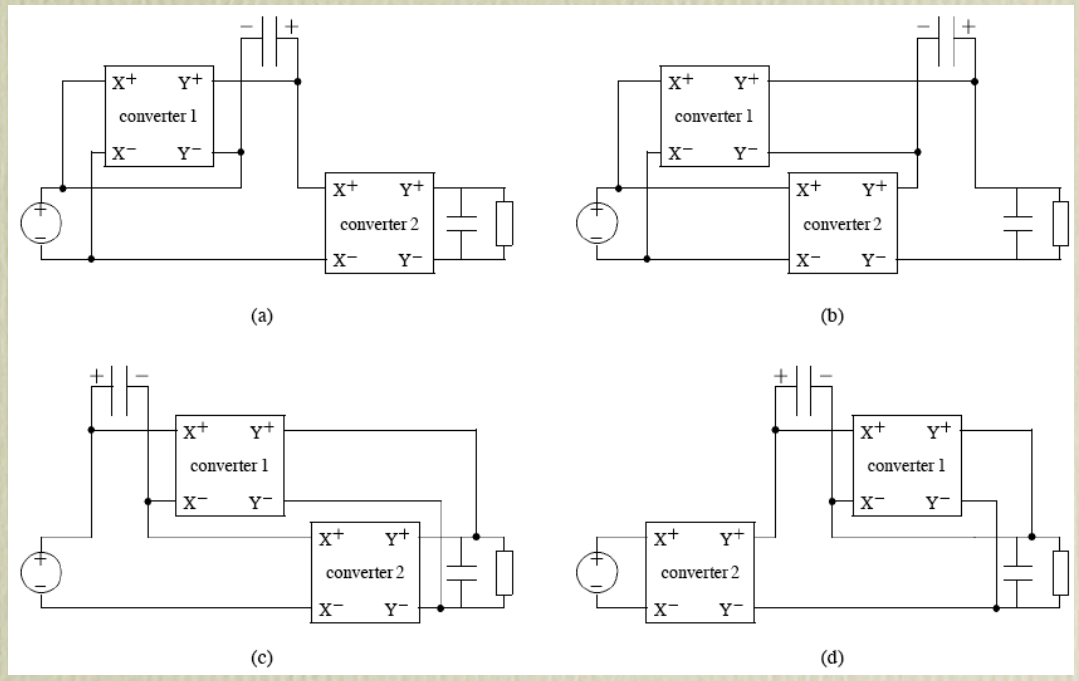
We consider the following basic converters to be inserted in any of the 16 structures.



Synthesis Procedure

For a detailed procedure, see
C. K. Tse, M. H. L. Chow and M. K. H. Cheung, "A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing," *IEEE Transactions on Power Electronics,* vol. 16, no. 6, pp. 794-802, November 2001. **(IEEE Transactions Best Paper Award Winner)**

In brief, we insert suitable converters in the respective positions (guided by certain circuit rules), and we will end up with a PFC voltage regulator of the desired characteristics.



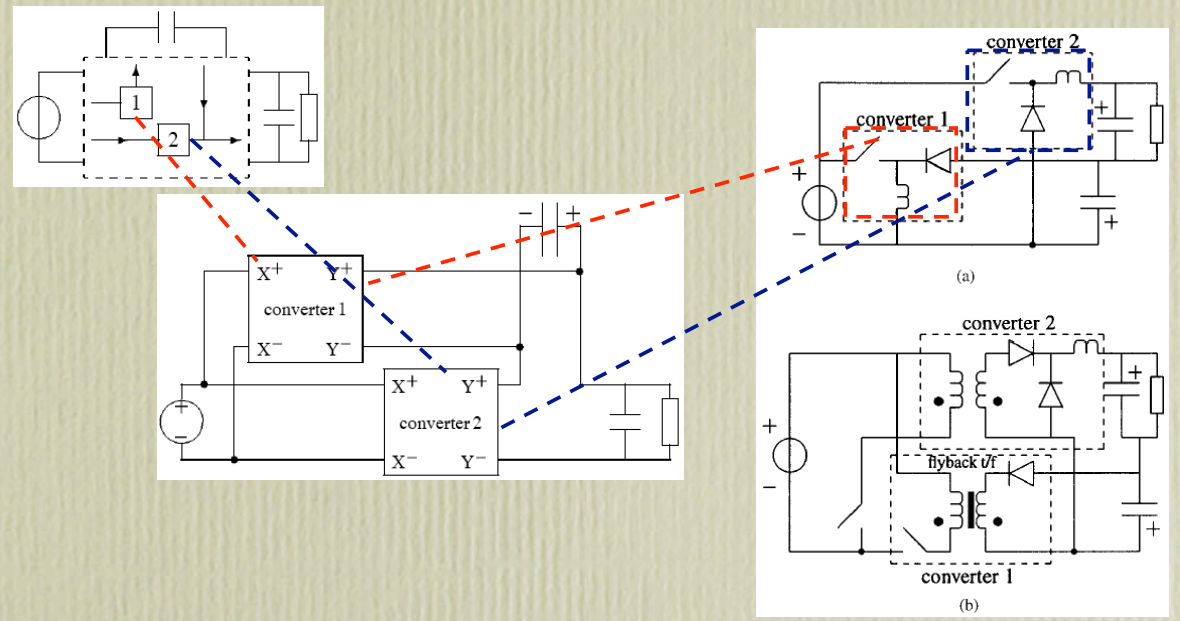
The Choice

It turns out that not all converters can be inserted. No free choice! This table shows the allowable configurations.

Configuration	Conv. 1	Conv. 2	Reported
I-IIA	buck–boost	buck	Zeta Chow *et al.* [20]
I-IIA	buck–boost	buck–boost	–
I-IIA	buck–boost	boost	–
I-IIB	buck	buck–boost	–
I-IIB	boost	buck–boost	–
I-IIB	buck–boost	buck	–
I-IIB	buck–boost	boost	–
I-IIIA	buck–boost	buck	–
I-IIIA	buck–boost	boost	–
I-IIIA	buck	buck–boost	–
I-IIIA	boost	buck–boost	–
I-IIIB	buck–boost	buck	–
I-IIIB	buck–boost	buck–boost	García *et al.* [19]
I-IIIB	buck–boost	boost	SEPIC BIFRED [5]

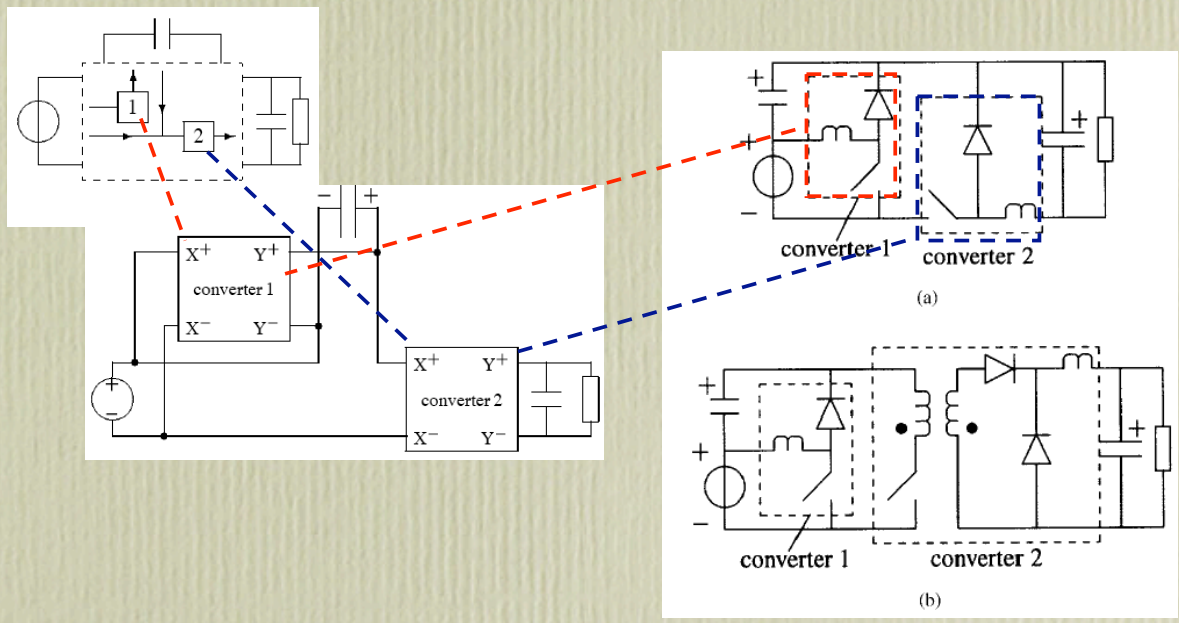
Synthesis Examples

Type I-IIB using a buck-boost and a buck converter.



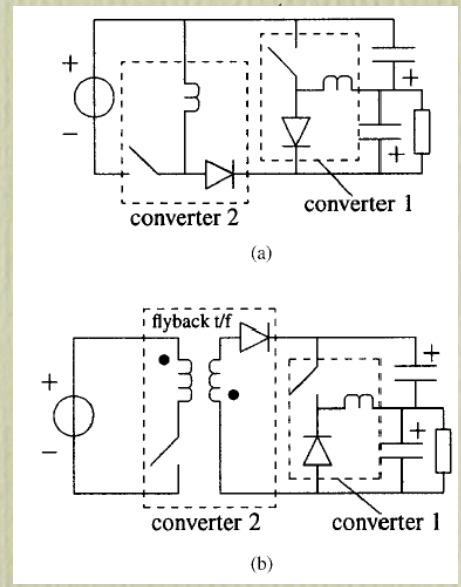
Synthesis Examples

Type I-IIA using a buck-boost and a buck converter.

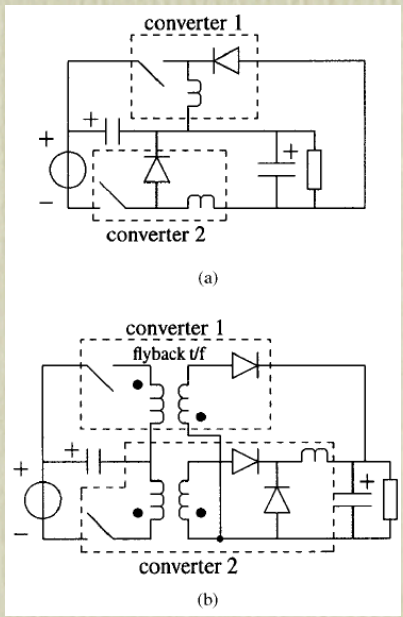


and more...

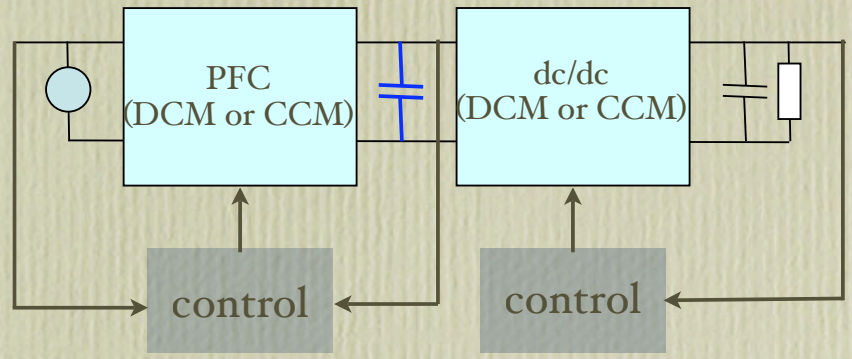
Type I-IIIB using buck-boost



Type I-IIIA using a buck-boost and a buck converter.



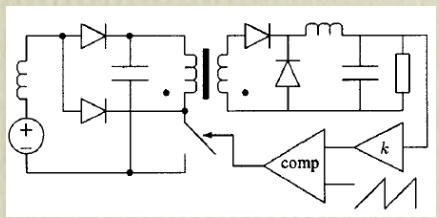
Control Problem



From formal theoretical study, we conclude that

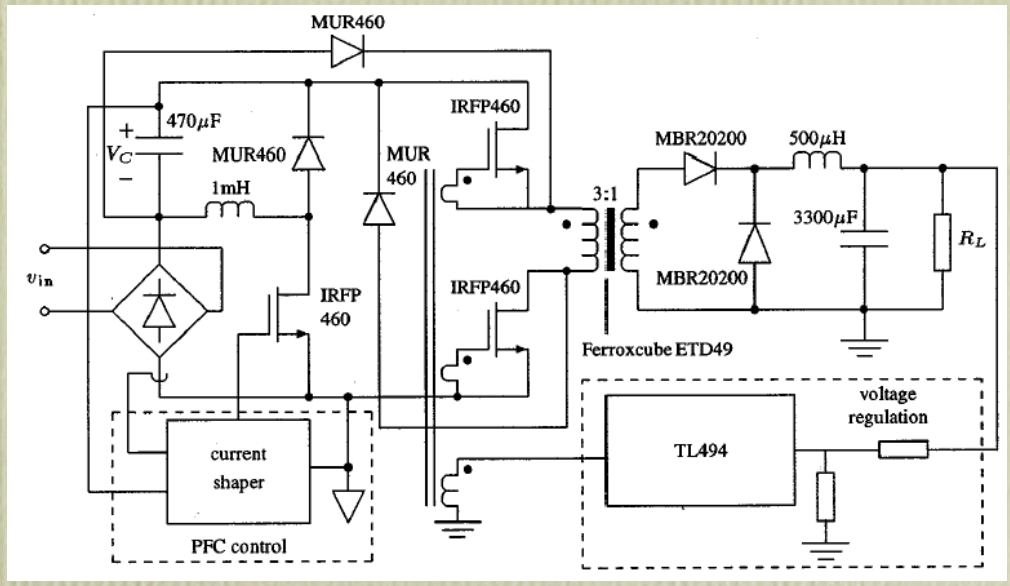
- In general we need TWO independent controls for full power control of two stages.
- For CCM-CCM, two duty cycles should be used.
- For DCM-CCM or CCM-DCM, frequency and duty cycle can be used
- Thus, single switch is possible if controls of *f* and *d* are properly designed
- Reasonable performance if only *d* control is used for cascade structure (shown by Redl *et al.* 1994)

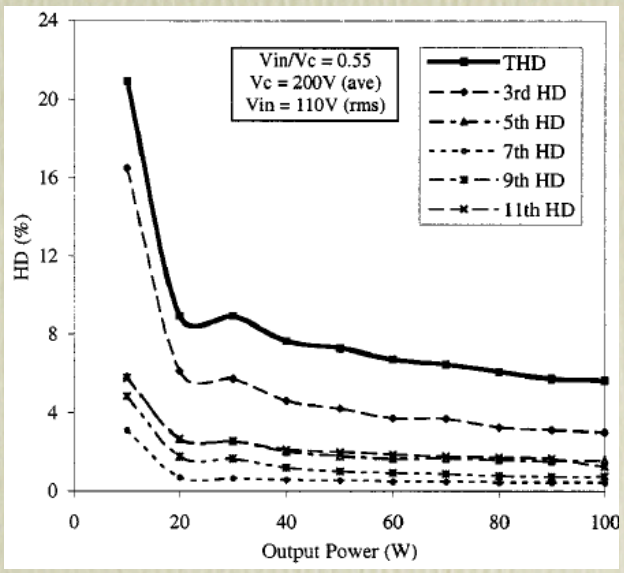
SSIPP by Redl *et al.*
(DCM-CCM or DCM-DCM)



Practical Design

Various configurations tested experimentally, e.g., see C. K. Tse, M. H. L. Chow and M. K. H. Cheung, "A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing," *IEEE Transactions on Power Electronics,* vol. 16, no. 6, pp. 794-802, November 2001.



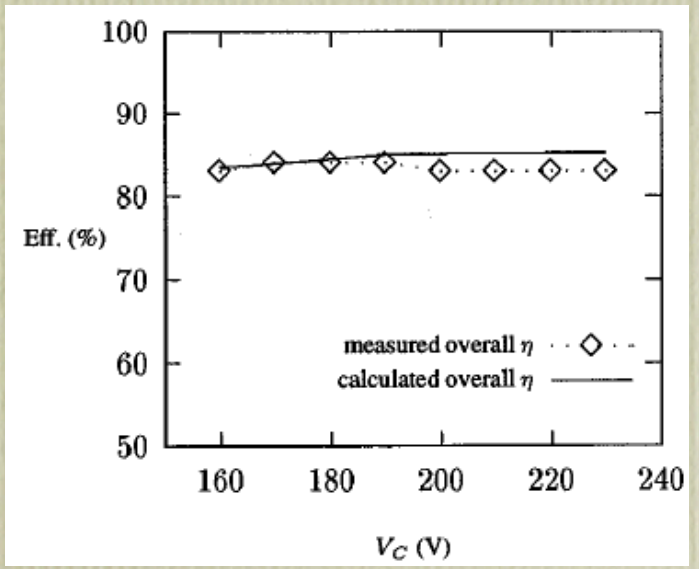


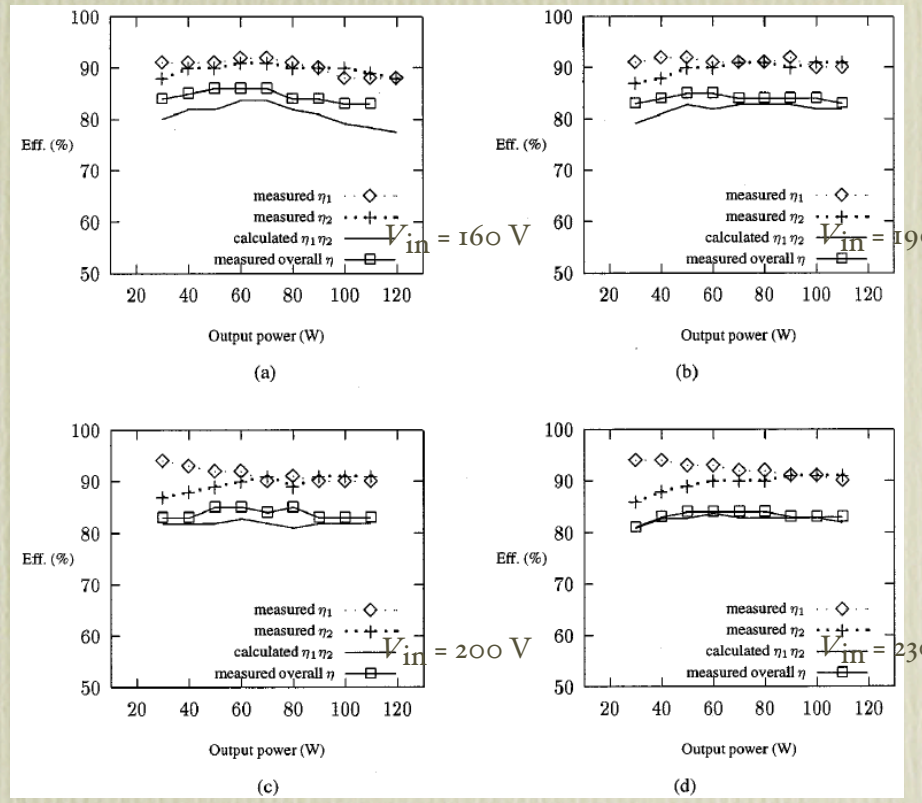
Efficiency "Claims"

Earlier on, we said that the non-cascade structure is supposed to be more efficient.

This is indeed true.

Note we are not interested in the absolute efficiencies, but rather look at the comparisons with the cascade structure!





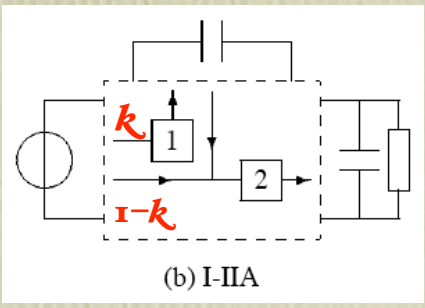
Some Unsolved Problems

We have seen the comparison of the cascade (type I-I) and non-cascade (all other types) structures.

All non-cascade structures involve a power split. **The design parameter is *k*.**

We observe that there is a trade off of PFC performance and efficiency. We mentioned (in slide #37) that the power split ratio *k* is important!

Can we optimize the design? What *k* gives best trade-off?



(b) I-IIA

Final Conclusion

The key point is that power factor correction and most other concepts are probably not new from the point of view of formal circuit theory. The question is *how the problem can be best understood from the basics*, and *then tackled in the best possible way.*

References

1. C. K. Tse, "Zero-order switching networks and their applications to power factor correction in switching converters," *IEEE Transactions on Circuits and Systems Part I,* vol. 44, no. 8, pp. 667-675, August 1997.
2. C. K. Tse and M. H. L. Chow, "Theoretical study of Switching Converters with Power Factor Correction and Voltage Regulation," *IEEE Transactions on Circuits and Systems I,* vol. 47, no. 7, pp. 1047-1055, July 2000.
3. C. K. Tse, M. H. L. Chow and M. K. H. Cheung, "A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing," *IEEE Transactions on Power Electronics,* vol. 16, no. 6, pp. 794-802, November 2001.
4. C. K. Tse, "Circuit Theory of Power Factor Correction in Switching Converters," *International Journal of Circuit Theory and Applications,* vol. 31, no. 1, 2003.
5. C. K. Tse, Y. M. Lai, R. J. Xie and M. H. L. Chow, "Application of Duality Principle to Synthesis of Single-Stage Power-Factor-Correction Voltage Regulators," *International Journal of Circuit Theory and Applications,* vol. 31, no. 6, pp. 555-570, November 2003.