Circuit Theory and Design of Power Factor Correction Power Supplies

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IEEE Distinguished Lecture 2005, Circuits and Systems
We will re-examine the concept of power factor correction (PFC), starting from the basics of circuit theory.

We will consider the fundamental requirements of PFC and how such requirements can be fulfilled.

We will develop systematic procedures for synthesizing PFC power supplies.
Introduction

• Efficient and compact power supplies are not priceless.
  – They present themselves as nonlinear loads to the mains, drawing current of distorted waveforms;
  – They generate noise that interferes other equipment and the environment

• Quantitative measures of power quality
  – Power factor / harmonic distortions
  – Radiated and conducted EMI
Power Factor

\[ p.f. = \frac{\text{Actual Power}}{VI \text{ Product}} = (\text{displacement factor})(\text{distortion factor}) \]

Phase shift between \( v \) and \( i \)  
Harmonic contents in \( i \)

Old concept of renewed interest

\[
\begin{align*}
p.f. &= \cos \phi \times \left( \sqrt{1 + \frac{(I_2/I_1)^2 + (I_3/I_1)^2 + \cdots}{\sqrt{1 + \text{THD}^2}}} \right) = \frac{\cos \phi}{\sqrt{1 + \text{THD}^2}}
\end{align*}
\]
Power Factor Correction

- Power converters are required to present themselves as linear resistance to the supply voltage. If the input voltage, $v$, is a sine wave, so is the input current, $i$. 

![Diagram of power factor correction technique with linear resistor](image)
The question is: How to make the converter look resistive?

- Composed of inductors and switches as seen from the mains;
- Operating with switches turned on and off at a frequency much higher than 50 Hz.
Hints

• The converter does not need to be resistive for all frequencies.
• If a filter is already there to remove switching frequency ripples, the converter needs only be resistive at low frequencies.

After all, **power factor correction is a low-frequency requirement.**
Destruction of Dynamics

Fundamental Properties

- Inductors cannot (are not allowed to) have “jump” current
- Capacitors cannot (are not allowed to) have “jump” voltage

![Diagram showing current and voltage force to zero periodically.](image)
Zero-order Inductors/ Capacitors

- Inductors forming a cutset with open switch(es) and/or current source(s) periodically
- Capacitors forming a loop with closed switch(es) and/or voltages source(s) periodically

\[ i_L = \text{zero periodically} \Rightarrow \text{no dynamics!} \]
Devoid of Dynamics

- Zero-order elements (Lo or Co) obviously do not store energy in a cycle, and hence are devoid of low-frequency dynamics. They can be considered as being resistive in the low-frequency range.
First Idea

• If the converter
  - contains only zero-order elements; and
  - the input does not “see” the output at all times,
• then the converter will look resistive to the input.
• Thus, we can make a PFC converter from this idea.
The “Perfect” Solution

Consider a flyback or buck-boost converter.

First, we can see that the input never “see” the output.

So, if we make the inductor zero-order by operating it in DCM, we have a resistive input.

Applying simple averaging, input resistance is

\[ R_{\text{in}} = \frac{2L}{D^2T} \]
A Not-So-“Perfect” Solution

Consider a **boost converter**.

Observe that the input sometimes “see” the output!!

Even if we make the inductor zero-order by operating it in **DCM**, we don’t precisely have a resistive input.

Applying simple averaging, input resistance is

\[
R_{\text{in}} = \frac{2L}{D^2T} \left(1 - \frac{V_{\text{in}}}{V_o}\right)
\]

forming cutset with open switches periodically by DCM operation

loop containing e and u
“Perfecting” It!

Consider a **boost converter** again.

If $D$ is reserved for other purposes, the $T$ must be varied to achieve “perfect” PFC, as in SSIPP*. (See Chow *et al.*, 1997)

It was also shown (Redl *et al.* and others) that even if no control is used, the power factor attained is still pretty “good”—good enough!

$$R_{\text{in}} = \frac{2L}{D^2T} \left( 1 - \frac{V_{\text{in}}}{V_o} \right)$$

*SSIPP—single-stage single-switch isolated PFC power supply*
What do we know now?

**Basic Criteria:**

- The DCM buck-boost or flyback converter satisfies the basic criteria of a “perfect” PFC. It thus naturally gives a good p.f.
- The DCM boost and buck converters are “not-so-perfect”, but can theoretically be perfected via feedback/ feedforward.

**Other Practical Considerations:**

- The DCM boost converter is preferred for its relatively better efficiency.
- Even under no control, the DCM boost converter has a pretty “good” p.f.
- The DCM buck converter is not preferred for its high peak current, and it suffers from the low voltage blackout (because it is a buck)!
Other Possibilities

Our fundamental criterion is

*Destruction of Dynamics of L and C!*

For voltage converters, the main constituent is the switching L. Therefore, our basic wish is to destroy the dynamics of the L in the converter.

We have shown how this destruction can be done by DCM operation. *What else can we do?*
Direct Destruction

Using direct current-programming, we can destroy the dynamics of the L. (The idea is that if we make the current dependent on the output voltage, it is no longer an independent variable, hence it is devoid of dynamics!)

Specifically, we program the current of L such that it assumes the wave shape that we want.
Second Idea

- CCM operation of the boost converter.
- Direct current programming such that its average (ripple removed) waveshape follows the input.
Standard IC Implementation

e.g., ACM PFC IC controller (see Wong, Tse & Tang in PESC2004)
Other Ideas

We have considered zero-order L.
How about zero-order C?
The problem (of course) is the basic restriction of
- the supply being a voltage
- the usual load requiring a voltage

(That’s why all converters are switching inductors in practice.)

Theoretically, switching capacitors are never excluded!
Duality Derivation

dual of DCM buck

dual of DCM buck-boost

dual of DCM boost
e.g. Duality Derived SSIPP

SSIPP based on boost + buck cascade

Numerous possibilities exist within this theoretical framework!
Practical PFC System

Always require tightly regulated DC output, in addition to PFC.

Can one converter do the jobs of PFC and tight output regulation?

No!

because we need a low-freq power buffer!
Power Buffer

In general we need a power buffer to achieve PFC and tight output regulation simultaneously.

3-port model

How many basic converters do we need?

Answer: TWO.
Two is enough!

We need two converters (arranged suitably, of course).

In fact, the so-called single-stage PFC regulator has two converter stages, strictly speaking. For example, the SSIPP is a boost converter plus a buck converter.

SSIPP by Redl et al.
A Different Question

Probably, the question of interest to the engineers is *HOW THE TWO CONVERTERS ARE POSSIBLY ARRANGED?*

**Best known configuration:**

![Diagram](attachment:image.png)
 Obviously, the problem of the cascade structure is the double processing of power in the two stages, degrading the efficiency.

Naturally, we wish to examine the way power is being processed.
Power Processing

Let’s start from the basics again.

In what ways power can flow within the 3-port model?
Power Processing

Let’s try fitting in the three types of flows.

Type I and Type I
Power Processing

Another try!

Type I, Type II
Power Processing

Another try!

Type I, Type III
Power Processing

Another try!

Type II, Type III
Power Processing Possibilities

To fulfill the power flow conditions of the 3-port model, we have 4 power flow possibilities.

(a) Type I-I  
(b) Type I-II  
(c) Type I-III  
(d) Type II-III
Completing the Structure

Finally, we place 1 converter to each path.
The Sixteen Configurations

Fitting in the two basic converters, we clearly see 16 possible structures.
Theoretical Efficiency

We can theoretically compare the efficiencies of the 16 structures. Obviously, the cascade (type I-I) is the poorest, and the others are always better since power is not doubly processed.

For example, consider the I-IIA structure. Suppose $k$ is the ratio of power split.

\[
\text{efficiency} = k\eta_1\eta_2 + (1-k)\eta_2
\]
\[
= \eta_1\eta_2 + (1-k)\eta_1(1-\eta_2)
\]
\[
> \eta_1\eta_2
\]

We shall see that this $k$ is a very important parameter. If $k$ is too large, the circuit resembles the cascade structure, hence no efficiency advantage. But if it is too small, P.F. degrades.
Theoretical Efficiency

We can theoretically compare the efficiencies of the 16 structures. Obviously, the cascade (type I-I) is the poorest, and the others are always better since power is not doubly processed.

<table>
<thead>
<tr>
<th>Config.</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-I</td>
<td>$\eta_1 \eta_2$</td>
</tr>
<tr>
<td>I-IA</td>
<td>$\eta_1 \eta_2 + (1-k)\eta_2(1-\eta_1)$</td>
</tr>
<tr>
<td>I-IIB</td>
<td>$k\eta_1 + (1-k)\eta_2$</td>
</tr>
<tr>
<td>I-IIC</td>
<td>$\eta_1 \eta_2 + (1-k)(1-\eta_1 \eta_2)$</td>
</tr>
<tr>
<td>I-III</td>
<td>$k\eta_1 + (1-k)\eta_2$</td>
</tr>
<tr>
<td>I-IIIIB</td>
<td>$\eta_1 \eta_2 + (1-k)\eta_2(1-\eta_1)$</td>
</tr>
<tr>
<td>I-IIIIC</td>
<td>$\eta_1 \eta_2 + (1-k)(1-\eta_1 \eta_2)$</td>
</tr>
<tr>
<td>II-A-III</td>
<td>$k\eta_1 + (1-k)\eta_2$</td>
</tr>
<tr>
<td>II-A-IIIIB</td>
<td>$\eta_1 \eta_2 + m(1-k)\eta_2(1-\eta_1) + k\eta_1 (1-\eta_2)$</td>
</tr>
<tr>
<td>II-A-IIIIC</td>
<td>$\eta_1 \eta_2 + m(1-k)(1-\eta_1 \eta_2) + k\eta_1 (1-\eta_2)$</td>
</tr>
<tr>
<td>II-B-III</td>
<td>$\eta_1 \eta_2 + m\frac{k}{\eta_1}(\frac{1}{\eta_2} - 1) + \left(\frac{(1-k)\eta_1 + k\eta_2}{\eta_1 \eta_2} - 1\right)$</td>
</tr>
<tr>
<td>II-B-IIIIB</td>
<td>$k\eta_1 + (1-k)\eta_2$</td>
</tr>
<tr>
<td>II-B-IIIIC</td>
<td>$\eta_1 \eta_2 + m\frac{k}{\eta_1}(\frac{1}{\eta_2} - 1) + \left(\frac{(1-k)\eta_1 + k\eta_2}{\eta_1 \eta_2} - 1\right)$</td>
</tr>
<tr>
<td>II-C-III</td>
<td>$\eta_1 \eta_2 + \eta_1 \eta_2 \left[ \frac{(1-k)\eta_2 + k\eta_1}{\eta_1 \eta_2} - 1 \right]$</td>
</tr>
<tr>
<td>II-C-IIIIB</td>
<td>$\eta_1 \eta_2 + \eta_1 \eta_2 \left[ k + \left(\frac{1-k}{\eta_2} + k\eta_1 \eta_2 \eta'' - 1\right) \right]$</td>
</tr>
<tr>
<td>II-C-IIIIC</td>
<td>$\eta_1 \eta_2 + (1-k)m(1-\eta_1 \eta_2)$</td>
</tr>
</tbody>
</table>

where $(1-k)\eta_2(1-\eta_1)>0$
where $k\eta_1 + (1-k)\eta_2 > \min\{\eta_1, \eta_2\} > \eta_1 \eta_2$
where $(1-k)(1-\eta_1 \eta_2)>0$
where $(1-k)(1-\eta_1 \eta_2)>0$
where $(1-k)(1-\eta_1 \eta_2)>0$
where $(1-k)(1-\eta_1 \eta_2)>0$
where $m(1-k)\eta_2(1-\eta_1) + k\eta_1 (1-\eta_2)>0$
where $m(1-k)(1-\eta_1 \eta_2) + k\eta_1 (1-\eta_2)>0$
where $(1-k)\eta_1 + k\eta_2 > \eta_1 \eta_2$ (see I-IIIB)
where $(1-k)\eta_1 + k\eta_2 > \eta_1 \eta_2$ (see I-IIIB)

where $\eta' = \frac{\eta_1 \eta_2}{(1-m)\eta_1 + m\eta_2}$ and $(1-k)\eta' + k\eta_1 \eta_2 > \eta_1 \eta_2 \eta''$
where $\eta'' = \eta_1 \eta_2$ and $(1-k)\eta_2 + k\eta'' > \eta_2 \eta''$
where $(1-k)(1-\eta_1 \eta_2)>0$
Comparing Efficiency

Note:

I don’t mean the above efficiency comparison is absolute! That will always put me in endless debate! You may have different efficiency optimization schemes for different stages, and in different forms.

So, why should I bother here?
Synthesis

The most important problem is **HOW TO CREATE CIRCUITS**.

We consider the following basic converters to be inserted in any of the 16 structures.
Synthesis Procedure


In brief, we insert suitable converters in the respective positions (guided by certain circuit rules), and we will end up with a PFC voltage regulator of the desired characteristics.
The Choice

It turns out that not all converters can be inserted. No free choice! This table shows the allowable configurations.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Conv. 1</th>
<th>Conv. 2</th>
<th>Reported</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-IIA</td>
<td>buck–boost</td>
<td>buck</td>
<td>Zeta Chow et al. [20]</td>
</tr>
<tr>
<td>I-IIA</td>
<td>buck–boost</td>
<td>buck–boost</td>
<td></td>
</tr>
<tr>
<td>I-IIA</td>
<td>buck–boost</td>
<td>boost</td>
<td></td>
</tr>
<tr>
<td>I-IIA</td>
<td>buck</td>
<td>buck–boost</td>
<td></td>
</tr>
<tr>
<td>I-IIA</td>
<td>boost</td>
<td>buck–boost</td>
<td></td>
</tr>
<tr>
<td>I-IIIB</td>
<td>buck–boost</td>
<td>buck</td>
<td></td>
</tr>
<tr>
<td>I-IIIB</td>
<td>buck–boost</td>
<td>boost</td>
<td></td>
</tr>
<tr>
<td>I-IIIB</td>
<td>buck–boost</td>
<td>buck–boost</td>
<td>Garcia et al. [19]</td>
</tr>
<tr>
<td>I-IIIB</td>
<td>buck</td>
<td>buck–boost</td>
<td>SEPIC</td>
</tr>
<tr>
<td>I-IIIB</td>
<td>boost</td>
<td>buck</td>
<td>BIFRED [5]</td>
</tr>
<tr>
<td>I-IIIB</td>
<td>buck–boost</td>
<td>boost</td>
<td></td>
</tr>
</tbody>
</table>
Synthesis Examples

Type I-II B using a buck-boost and a buck converter.
Synthesis Examples

Type I-IIA using a buck-boost and a buck converter.
and more...

Type I-IIIB using buck-boost

Type I-IIIA using a buck-boost and a buck converter.
From formal theoretical study, we conclude that

- In general we need TWO independent controls for full power control of two stages.
- For CCM-CCM, two duty cycles should be used.
- For DCM-CCM or CCM-DCM, frequency and duty cycle can be used.
- Thus, single switch is possible if controls of $f$ and $d$ are properly designed.
- Reasonable performance if only $d$ control is used for cascade structure (shown by Redl et al. 1994)
Practical Design

Efficiency “Claims”

Earlier on, we said that the non-cascade structure is supposed to be more efficient.

This is indeed true.
Note we are not interested in the absolute efficiencies, but rather look at the comparisons with the cascade structure!
Some Unsolved Problems

We have seen the comparison of the cascade (type I-I) and non-cascade (all other types) structures.

All non-cascade structures involve a power split. **The design parameter is \( k \).**

We observe that there is a trade off of PFC performance and efficiency. We mentioned (in slide #37) that the power split ratio \( k \) is important!

Can we optimize the design? What \( k \) gives best trade-off?
Final Conclusion

The key point is that power factor correction and most other concepts are probably not new from the point of view of formal circuit theory. The question is how the problem can be best understood from the basics, and then tackled in the best possible way.


