HIGH FREQUENCY FILTER DESIGN

for
High-Frequency Circuit Design Elective

by
Michael Tse

September 2003
<table>
<thead>
<tr>
<th>CONTENTS</th>
</tr>
</thead>
</table>
| 1. **Introduction** | 1.1 Types of filters  
| | 1.2 Monolithic filters  
| | 1.3 Integrators  
| | 1.4 Simple first-order gm-C filters  
| 2. *Filter Design for High Frequencies* | 2.0 Introduction to filters (separate notes)  
| | 2.1 Special requirements for HF  
| 3. **Gm-C Filter Synthesis** | 3.1 Cascaded biquads  
| | 3.2 Signal flow graphs  
| 4. **Realization of Transconductors** | 4.1 BJT transconductors  
| | 4.2 MOSFET transconductors  
| | 4.3 Exercise  

---

Michael Tse: HF Filter Design
1. INTRODUCTION

1920
- Basic forms: LC-Ladders

1960
- Due to the advent of op-amps, “ACTIVE RC” filters became popular.
- Miniaturization leads to IC filters which use monolithic technology for active components and thin-films for frequency determining components (C,R).

1970
- IC monolithic filters became popular.
  - Advantages:
    - Less components, smaller volume
    - Good matching of components
    - Automatic tuning – correct transfer functions for process/temp variations
    - Smaller parasitic caps on chip
    - Fabricated in large quantity
1.1 Types of Filter Realizations

- Digital filters
- Analog discrete-time filters
- Analog continuous-time filters

1.1.1 Digital filters:
Signals need to be discretized and digitized, i.e., sampled and converted to digital words, and the filtering is done in the digital domain.

1.1.2 Analog discrete-time filters
Signals are discretized but NOT digitized. They are called sampled-data. Filtering is done directly to the sampled-data.
Example: switched-capacitor filters (SC filters)
But SC filters are mainly for low-frequency applications (audio range)

Michael Tse: HF Filter Design
1.1.3 Analog continuous-time filters

Continuous analog signals are directly processed without any A/D or D/A conversions, sampled-&-hold, anti-aliasing filters, etc. Because of the continuous-time nature, analog continuous-time filters are very suitable for high-frequency and high dynamic range applications.

Disadvantages:

1. Sensitive to process and temperature variations
2. Aging
3. Need tunings of the frequency determining components

Since we are dealing with high-frequency design, we will focus on Analog Continuous-time Filters in these notes.
1.2 Monolithic Filters

Fully integrated analog continuous-time filters were possible when automatic tuning of components became available, starting 1970’s.

1.2.1 Bipolar filters

- High voltage gain
- High output drive
- High frequency (up to ~100 MHz)
- Low noise and offsets

1.2.2 MOS filters

- Low power
- High packing density
- High noise immunity
- Ease of design
- Ease of scaling
- High frequency (up to ~100 MHz)
1.3 Integrators (Building Blocks)

Integrators are needed in all active filters. [In passive filters, integrators are provided by inductors and capacitors, in both I and V domains.]

However, for active filters, only \( C \) exists. Hence, we need to have integrators of output/input variables are in the same voltage or current domain.

1.3.1 Active RC (Op-amp RC) Integrators

\[
V_o = \sum_{i=1}^{n} \frac{V_i}{C_{int}R_i} \sum_{j=1}^{m} \frac{C_jV_j}{C_{int}}
\]

mosfet in triode region to simulate a resistance

Michael Tse: HF Filter Design
Active RC Integrators (con’t)

The RC integrator shown previously is not very suitable for monolithic realization because the time constant $t = R \cdot C_{int}$ cannot be tuned after realization!

Note that C and R can only be fabricated with an accuracy of 20% and 5% respectively.

With MOSFET-C integrators, the tuning problem can be solved by varying the gate voltage of $M_i$

$\rightarrow R_i \rightarrow \big[ \big].$

Design notes:

1. Nonlinearity of MOSFETS is mainly second-order. Thus, MOSFET-C integrators must be designed in BALANCED FORM in order to cancel even harmonics.

2. It is difficult to implement good MOS op-amps. Usually, BiMOS technology is used for MOSFET-C integrator filters.

3. It is also possible to tune the frequency using the transconductance instead of the MOSFET resistance.
1.3.2 Transconductance-C or gm-C Filters

The general gm-C integrator:

We can control $t_i = C_{eff}/g_m$ by tuning the transconductance. Note: The transfer function suffers from loading effects, which depend on the summation cap $C_j$.

The gain $g_m$ is a design parameter (whereas in active-RC, the op-amp gain doesn’t matter).

$$V_o = \sum_{i=1}^{n} \frac{g_{m_i}V_i}{\sum_{j=1}^{m} \frac{C_jV_j}{C_{eff}}} + \sum_{j=1}^{m} \frac{C_jV_j}{C_{eff}}$$

where $C_{eff} = C_{int} + \sum_{j=1}^{m} C_j$
1.4 Simple First-order gm-C Filters

The basic transfer function is: \[ H(s) = \frac{V_{out}}{V_{in}} = \frac{k_1 s + k_0}{s + w_0} \]

Gm-C realisation:

The nodal equation is:

\[ g_{m1} V_{in} + s C_X (V_{in} - V_{out}) s C_A V_{out} - g_{m2} V_{out} = 0 \]

\[ V_{out} \]

\[ V_{in} \]

The parameters are adjusted by

\[ C_X = \frac{k_1 C_A}{1 - k_1} \] for \( 0 \leq k_1 < 1 \)

\[ g_{m1} = k_0 (C_A + C_X) \]

\[ g_{m2} = w_0 (C_A + C_X) \]
2 FILTER DESIGN FOR HIGH FREQUENCIES

2.1 Special Requirements for HF

(a) No nodes with an undesired capacitance to ground.

In VHF, parasitic caps become significant and quite similar values to the designed capacitances. Thus, we need to make sure that each node in the filter MUST have a desired capacitance to ground so that we know what it is and how it is put in the transfer functions.
2.1 Special Requirements for HF (con’t)

(b) Balanced operation for reducing even harmonics and crosstalks. Signal inversion can be obtained easily in gm-C.

Balanced transconductance:

\[ V_c + \frac{1}{2} V_{\text{in}} \]

\[ V_c - \frac{1}{2} V_{\text{in}} \]

\[ I_{\text{out, diff}} = I_{\text{op}} - I_{\text{on}} = g_m V_{\text{in}} \]

\[ I_{\text{op}} = + \frac{g_m V_{\text{in}}}{2} \]

\[ I_{\text{on}} = - \frac{g_m V_{\text{in}}}{2} \]
2.1 Special Requirements for HF (con’t)

(c) Sensitivity must be LOW for component variations to reduce errors.

In VHF filters, the capacitors are small and will have 20-100% part of parasitic cap. Hence, inaccuracy is expected in capacitance ratios. Fortunately, ratios of gm are usually integer numbers, matching between gm’s should be good. Thus, sensitivities of filter transfer functions to capacitor values MUST BE KEPT LOW.

(d) Dynamic range is determined by

• dynamic range of gm
• dynamic range of filter structure

e.g., if internal node signal levels have large variations (swings), then the output swing becomes restricted. This usually requires computer simulations for optimisation.
3. Gm-C FILTER SYNTHESIS

1. Cascaded biquad
2. Signal flow graph
3. State space method
4. Gyrator method

BIQUAD: circuit realizing a general filter transfer function of second order

\[ H(s) = K \frac{a_2 s^2 + a_1 s + a_0}{s^2 + s \frac{\omega_o}{Q_p} + \omega_o} \]

- \(a_2 = a_1 = 0\) --> LOWPASS
- \(a_2 = a_0 = 0\) --> BANDPASS
- \(a_1 = a_0 = 0\) --> HIGHPASS
- \(a_1 = 0\) --> BANDSTOP
3.1 Cascaded Biquads

General biquad section using gm-C realization (VHF applications)

\[ V_o = \frac{C_3}{C_2 + C_3} \frac{s^2 V_c + s \frac{g_m}{C_3} V_b + \frac{g_m}{C_1} V_a}{s^2 + s \frac{g_m}{C_2 + C_3} + \frac{g_m}{C_1} \frac{g_m}{C_2 + C_3}} \]

where \( Q_o = \sqrt{\frac{g_m g_m}{C_1 (C_1 + C_2)}} \)

\[ Q_p = \sqrt{\frac{C_2 + C_3}{C_1} \frac{g_m g_m}{g_m}} \]

So, \( K, a_0, a_1, Q_o \) and \( Q_p \) can be chosen by choosing gm’s and C’s.
3.1 Cascaded Biquads (con’t)

Features:
1. This biquad is suitable for *very high frequencies* because each node has a known capacitance to ground.
2. $C_2$ is *not essential, but is unavoidable*. Hence, it must be taken into account.
3. Cascading multiple biquads will *cause loading effects*, which must be taken into consideration because there is no ideal buffer at high frequencies.
4. Output level can be scaled for optimal dynamic range by varying $K$.

High order filters:

Disadvantage of cascaded biquads:
Passband sensitivity to component variations tends to be too large for some applications. (A better approach is to start with LC ladder.)
3.2 Signal Flow Graph Synthesis

The starting point is passive lossless LC ladder. The following is a 3rd order elliptic low-pass filter.

The state equations:

State $V_{C2}$:  
\[ sC_2V_{C2} + I_{L3} + I_{C3} = I_1 \]

\[ sC_2V_{C2} + I_{L3} + sC_3(V_{C2} \square V_{C4}) = \frac{V_{in} \square V_{C2}}{R_1} \]

\[ (sC_2 + sC_3)V_{C2} \square sC_3V_{C4} + \frac{V_{C2}}{R_1} = \frac{V_{in}}{R_1} \square I_{L3} \]

\[ V_{C2} + \frac{V_{C2}}{s(C_2 + C_3)R_1} = \frac{C_3V_{C4}}{C_2 + C_3} + \frac{V_{in}}{sR_1(C_1 + C_3)} \square \frac{I_{L3}}{s(C_2 + C_3)} \]
3.2 Signal Flow Graph Synthesis (con’t)

Signal flow graph for state $V_{C2}$:

Combining similar factors together
3.2 Signal Flow Graph Synthesis (con’t)

State $V_{C4}$:

\[
sC_4 V_{C4} + \frac{V_{out}}{R_5} = I_{L3} + sC_3 (V_{C2} \square V_{C4})
\]

\[
s(C_4 + C_3) V_{C4} = \frac{\square V_{out}}{R_5} + I_{L3} + sC_3 V_{C2}
\]

\[
V_{C4} = \frac{\square V_{out}}{sR_5 (C_3 + C_4)} + \frac{I_{L3}}{s(C_3 + C_4)} + \frac{C_3 V_{C2}}{C_3 + C_4}
\]
3.2 Signal Flow Graph Synthesis (con’t)

State $I_{L3}$:

\[ sL_3 I_{L3} = V_{C2} - V_{C4} \]

\[ I_{L3} = \frac{V_{C2} - V_{C4}}{sL_3} \]
Combining the three sub-graph, we get the final signal flow graph:

\[ R_1 I_{L3} \quad R_1 = R_5 \]
3.2 Signal Flow Graph Synthesis (con’t)

We can now synthesize the circuit with gm-C. The rules are:

1. The “1” branch is gm.
2. All transconductances are $1/R_1$.
3. $1/s$ branch is cap to ground.
4. Gains $C_3/(C_2+C_3)$ and $C_3/(C_4+C_3)$ can be realized by capacitor ladder.

Exercise: Convert it to a balanced gm-C circuit.
4. REALISATION OF TRANSCONDUCTORS

Transconductors (gm blocks) can be realized in BJT form or MOSFET form.

**Bipolar:**

1. Fixed transconductor cascaded with gain cell. A fixed transconductor is usually a differential pair linearized by resistor degeneration.

2. Differential input stage with multiple inputs, with transistor scaling for better linearity.

**MOS:**

1. Fixed-bias triode MOS transistor as resistor. Multiple outputs are possible using mirrors.

2. Varying-bias triode MOS transistor as resistor.

3. Differential input with constant drain-source current.

To avoid confusion, in the next pages, we use $G_m$ to stand for the transconductance of the whole block, and $g_m$ for the transistor’s.
4.1 BJT Transconductors

Fixed transconductance using resistor

\[
\frac{i_{o1}}{V_i} = G_m = \frac{1}{\frac{2}{g_m} + R_E}
\]

**Note:**
Distortion due to non-constant \(G_m\). So, linearity can be improved if \(R_E\) is much greater than \(1/g_m\) of the transistor. Moreover, if \(V_{be}\) is assumed fixed, \(V_i\) appears purely across resistor and hence \(G_m = 1/R_E\) (independent of \(g_m\)).
4.1 BJT Transconductors (con’t)

Finding the $G_m$ for this fixed transconductance

Half-circuit equivalent model:

$$i_{o1} = g_m \frac{V_i}{2} + \frac{r_\pi}{r_\pi + \frac{R_E}{2}} = V_i \frac{1}{2g_m + R_E}$$

$$\frac{i_{o1}}{V_i} = G_m = \frac{1}{2 + \frac{R_E}{g_m}}$$
4.1 BJT Transconductors (con’t)

Gain-cell transconductor (tunable $G_m$)

The transconductance can be tuned by setting the current ratio $I_2/I_1$. 

\[
G_m = \frac{1}{R_E} \begin{bmatrix} I_2 \\ I_1 \end{bmatrix}
\]
4.2 MOSFET Transconductors

Fixed-bias triode MOSFET—using a MOSFET operating in triode region to simulate a resistor

\[ G_m = \frac{i_{o1}}{V_i} = \frac{W}{L} C_{ox} (v_{gs9} - V_{TH}) \]

Transconductance is

This \( G_m \) can be easily modified to give multiple outputs! (using mirrors)
Varying bias triode MOSFET—improved linearity

Q3 and Q4 are in triode region and undergo varying bias conditions (because their gates are not connected to fixed bias.) Why is linearity improved? Try the exercise on next page.

Transconductance is

$$G_m = \frac{i_{o1}}{V_1 Q_1 V_2 Q_2} = \frac{4k_1 k_3 \sqrt{I_1}}{(k_1 + 4k_3) \sqrt{k_1}}$$

where $k_n = \frac{C_{ox}}{2} \frac{W}{L \sqrt{n}}$
EXERCISE

Consider the circuit of the previous page. Suppose $I_1 = 100\mu A$, $\mu C_{ox} = 96\mu A/V2$, $(W/L)_1 = (W/L)_2 = 20$, $(W/L)_3 = 3$, and $V_2 = 0$.

(a) Assuming a perfectly linear transconductor, find $i_{o1}$ when $V_1=2.5mV$ and 250mV, using the formula given in the previous page.

(b) Assume the gates of $Q_3$ and $Q_4$ are connected to ground and use classical models for both the triode and active regions. Find the true value of $i_{o1}$ when $V_1=2.5mV$ and 250mV. Compare your results with those found in (a).

(c) Repeat (b), assuming the gates of $Q_3$ and $Q_4$ are connected to the input signals as shown in the circuit.

(d) Comment on the linearity improvement, if any, when varying bias triode transistor is used.